Analysis and Modeling of a Low Voltage Triggered SCR ESD Protection Clamp with the Very Fast Transmission Line Pulse Measurement

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Abstract

The analysis and the modeling of a Low Voltage Triggered SCR (Silicon Controlled Rectifier) under vf-TLP (very-fast Transmission Line Pulse) measurements are reported. The results measured by vf-TLP system showed that the triggering voltage (Vt1) decreased and the second breakdown current (It2) increased in the comparison with the results measured by a standard 100ns TLP (Transmission Line Pulse) system. A compact model based on the vf-TLP measured characteristics is presented. The measurement result and the simulation data of the behavior approached model indicate a good correlation.

Keywords

ElectroStatic Discharge (ESD), Silicon Controlled Rectifier, Very Fast Transmission Line Pulse Measurement, compact model

1. Introduction

Electrostatic Discharge (ESD) protection has become an important task in the pursuit of increasing the reliability of semiconductor ICs [1]–[4]. Furthermore, ESD stress caused by the Charged Device Model (CDM) gains more and more attention in the semiconductor industry. It is because the technology scaling has brought lower two breakdown voltages; gate oxide breakdown and drain-source breakdown in CMOS FETs. Under 130 nm, these breakdown voltages fall below 10V for the transient stresses which is occurred in short duration (~1ns) by CDM discharges [5]. All these trends make the job, which is ensuring adequate ESD protection, more challengeable in 130 nm than in previous technology generations.

Moreover, contrary to the HBM (Human Body Model), device physics regarding the CDM are still not well known. It is because the proper measuring equipments have not been developed yet. However, in the meantime, the vf-TLP system can be used to measure the behavior of DUT (Device Under Test) in the transient stress like CDM discharges. This vf-TLP system can generate a pulse with around 100 ps rise time and 1 ns width [6]. The time scale of this pulse characteristic is similar to that of the CDM stress. The vf-TLP system is used to construct the high-current I-V characteristics of protection elements, just as standard TLP system does. Hence, the behavior of protection elements under CDM stress conditions can be studied by the vf-TLP test.

In this paper, we investigated the characteristic of the Low Voltage Triggered SCR (LVTSCR) which is widely used as the CDM protection device. The LVTSCR is a well-known ESD clamp for the CDM protection since it has the low triggering voltage characteristic and the high current capability within the relative small size. To begin with, we investigated the characterization and the behavior of a LVTSCR fabricated in a 0.13μm CMOS process using the 100ns standard TLP system and the 1.2ns vf-TLP. The results measured by a vf-TLP system showed that the triggering voltage (Vt1) decreased and the second breakdown current (It2) increased in the comparison with the results measured by a standard 100ns TLP system. A series of experiments proved that it comes from the dV/dt effect and the power-to-failure with the pulse width.

In addition, we present a compact model of the LVTSCR based on the vf-TLP measured characteristics. The triggering voltage (Vt1), the holding voltage (Vh), and the on-resistance (Ron) are extracted by the vf-TLP measurement. These key parameters are used for the behavior modeling.

2. Low Voltage Triggered SCR (LVTSCR)

A low voltage triggered SCR (LVTSCR) device implemented in a 130nm RF process is studied in this paper. The LVTSCR is a well-known ESD protection structure with the low voltage triggering characteristics and the area-efficiency [7], [8]. Generally, SCR devices have much higher ESD robustness than other ESD devices such as diodes and ggNMOS (grounded-gate NMOS) [9]. Accordingly, the ESD clamp which uses this SCR device is relative small size and then makes less parasitic capacitance. However, conventional SCR devices have the high triggering voltage which is generally greater than the gate-oxide breakdown voltage of the input stages. Therefore, normal SCR device is not suitable for the input CDM protection clamp without improving the triggering characteristics whereas the LVTSCR overcame this high triggering voltage problem using the embedded ggNMOS (grounded-gate NMOS). As this advantage, the LVTSCR is widely used for the input CDM protection. The operating mechanism of the LVTSCR is given below

In the ESD event, the ggNMOS turns on first, and then it makes the substrate current. Finally, this substrate current induces the SCR to operate. Figure 1 shows the cross-sectional view of the LVTSCR device. The LVTSCR consists of a PNP bipolar formed by the P+, Nwell of the cathode region, P-substrate, and an NPN formed by the N+, Pwell of the anode region, and the Nwell of the cathode region. In addition, the ggNMOS is embedded to reduce the triggering voltage. Hence, the LVTSCR operates like the ggNMOS at the low current regime, and SCR at the high

current regime. Thus, using a LVTSCR device for the input CDM protection can achieve better CDM performances.

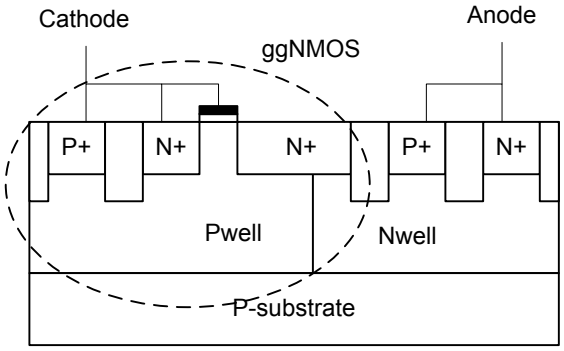

Figure 1: The cross-sectional view of the LVTSCR device

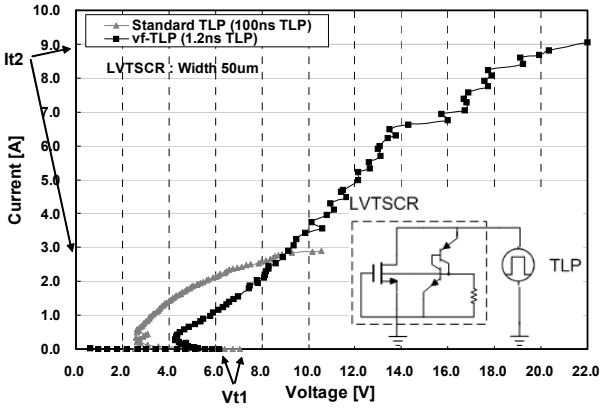

Figure 2: The high-current I-V characteristics of the LVTSCR device measured by the 100ns standard TLP and the 1.2ns vf-TLP system

3. Measurements and Analysis

The LVTSCR device was implemented with G-S-G (Ground-Signal-Ground) pads to measure the on-wafer I-V curve using the vf-TLP system. The performance of the vf-TLP system is often limited by the type of probes which deliver the pulse to wafer. Because of the narrow width pulse (~1ns) used in the vf-TLP system, the wafer probes must have high frequency performance characteristics.

Figure 2 shows the high-current I-V characteristics of the LVTSCR device of 50μm widths measured by a 100ns standard TLP system and a 1.2ns vf-TLP system. In the comparison with the I-V characteristics by the standard TLP system, the I-V characteristics measured by vf-TLP have two differences. To begin with, the triggering voltage (Vt1) is decreased. In addition, the second-breakdown current (It2) is increased.

3.1 The dV/dt effect

The lower Vt1 is caused by 'the dV/dt effect' [10]. When a fast ESD transient current is applied to the device, the triggering ability is enhanced. It is because more base current, which is induced by the fast ESD transient current, can easily turn on the parasitic bipolar. Accordingly, the triggering ability of the LVTSCR is largely enhanced, and then the triggering voltage is deceased. It means that this device needs relatively low voltages to turn on the parasitic NPN in the condition of the fast rise time (around 100 ps).

The very fast rise time reduces the Vt1, triggering voltage shown on the Figure 3, where the Vt1 decreases by around 1 volt with a 137ps rise time due to the dV/dt effect. A fast ESD transient, which has the high applied dI/dt, will generate a high dV/dt over the drain bulk junction capacitance and increase the bulk potential by a displacement current. The displacement current is flows through the drain-bulk junction for a short period of time. Thus, fewer avalanches current is needed to provide base bias which triggers the parasitic NPN. The effective Vt1 can be reduced significantly below the junction breakdown. Figure 4 shows the effect of the dV/dt in a LVTSCR.

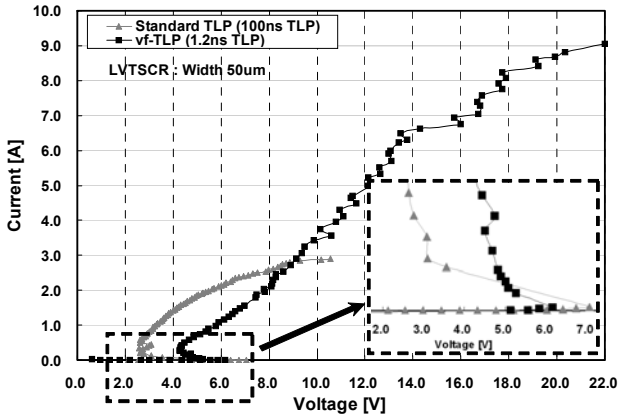

Figure 3: The high-current I-V characteristics of the LVTSCR device measured by the 100ns standard TLP system and 1.2ns vf-TLP systems and the enlargement of the TLP-measured I-V curve at the triggering regime

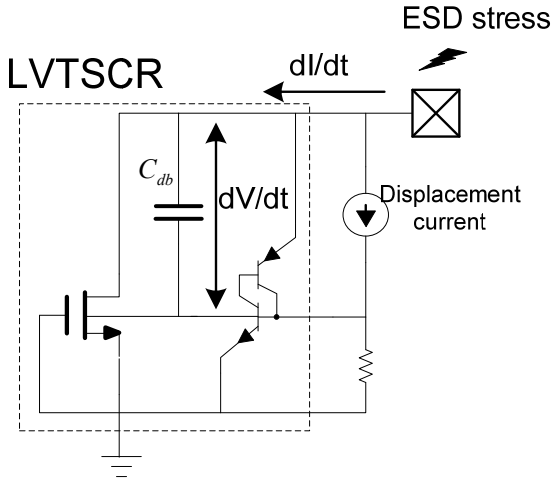

Figure 4: The very fast rise time generates a high dV/dt (dI/dt). It makes the high displacement current and this allows the low triggering voltage

3.2 The P_f versus τ relationship

The main reason of the failures caused by the ESD is the thermal heating. In this sense, the factor, how long the ESD pulse stresses the device, is important to expect the robustness of ESD protection circuits. The prior research explained well that the failure of semiconductor devices can

be understood from a universal curve where P_f plotted versus pulse width τ , and this curve is called as the Wunsch-Bell curve [11].

Figure 5 shows an illustrative Wunsch-Bell curve. The Wunsch-Bell curve explains the relationship between physical failure and a melting temperature. It also addresses the relationship between the heat transfer time constant and the applied pulse width. The relationship is that the longer pulse makes the ESD robustness reduced.

Figure 6 shows the I-V results with different pulse widths. This I-V curve is well agreed with a Wunsch-Bell's explanation. The second-breakdown current for the 1.2ns pulse is approximately 3A higher than the measurement with the 5ns pulse. The It2 level is increased linearly by decreasing the pulse width (5ns, 2.5ns, and 1.2ns). It can explain well why the It2 measured by the vf-TLP system is higher, in comparison with the It2 measured by the standard TLP system.

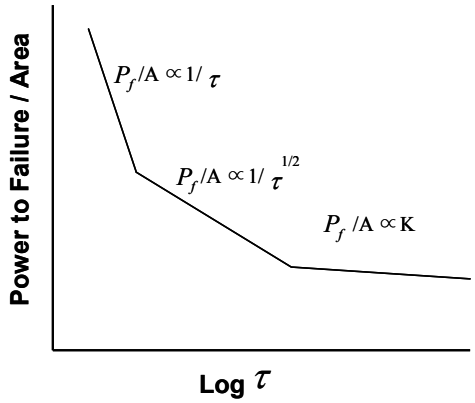

Figure 5: The Wunsch-Bell curve: the power-to-failure per area versus logarithm pulse width [11].

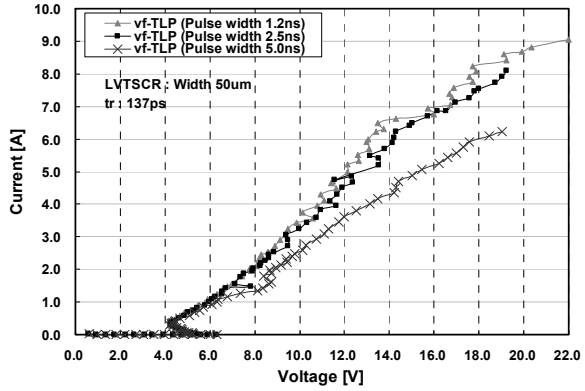

Figure 6: The comparisons of the vf-TLP measured I-V curves with three different pulse widths (1.2ns, 2.5ns, and 5.0ns)

Table 1 shows the compared results of the second-breakdown current (It2) with different pulse widths. The second-breakdown (or failure) current in Table1 is increased linearly by decreasing the pulse width again.

Table 1: Comparisons of the second breakdown current between the 100ns standard TLP and the vf-TLP with three different pulse widths (100ns, 5.0ns, and 2.5ns)

	Standard TLP	**vf-TLP**		
Pulse width [ns]	100	5.0	2.5	1.2
It2 (Second Breakdown current) [A]	2.9	6.1	7.9	8.8

4. Compact model

As stated above, the vf-TLP measured characteristics of the LVTSCR come from the dV/dt effect and the power-to-failure with the pulse widths. The triggering voltage (Vt1) decreases by around 1 volt, and the second-breakdown current (It2) for the 1.2ns pulse is approximately 6A higher than the measurement with the standard TLP tester. Table 2 shows the key design parameters which are extracted by the vf-TLP measurements with 137ps rising time and 1.25ns pulse width.

In this work, we approached the macro-modeling method. It allows reusing the model of the NMOS and the bipolar transistor from the standard model library, which is provided by the foundry. These key design parameters extracted by the vf-TLP system.

Table 2: Extracted key parameters of the LVTSCR under the vf-TLP system (rising time: 137ps, pulse width: 1.25ns)

	vf-TLP measured results
Vt1 (Triggering voltage) [V]	6.2
Vh (Holding voltage) [V]	4.3
Ron (on-resistance) [Ω]	1.9
It2 (Second Breakdown current) [A]	8.8

The equivalent circuit of this LVTSCR device, which consists of a PNP and a NPN bipolar transistor with the ggNMOS for the low voltage triggering, is shown in Figure 7. Due to the reverse-biased junction between the N- and P-well regions, the SCR device is turned off under normal circuit operating conditions. When a positive ESD stress is zapped from the anode to the grounded cathode, the high voltage drop between the anode and cathode causes breakdown on the base–collector junction of the parasitic BJT which is formed under the ggNMOS. In the meantime, the PNP and NPN transistors will be turned on by this breakdown current from the parasitic BJT under the ggNMOS.

The behavior model of the LVTSCR is formed by adding a ggNMOS device to the SCR model, as shown in Figure 7. The equivalent Pwell and Nwell resistance, Rpw and Rnw, are used to control the activation and the high-current operation of the equivalent SCR device. Other electrical parameters of two bipolar devices were brought from the standard model library which is provided by the foundry. There is no additional physical model in this behavior model

except the models provided by the foundry. The goal of this ESD compact model is to provide circuit designers a means of verifying their ESD protection strategy while monitoring the impact of the ESD protection structures on the circuit performance.

We used the transient mode of the HSPICE simulation for simulating the vf-TLP system [12]. The vf-TLP system generates the rectangular waveform which has the 100 ps rising time and the 1ns pulse width. This pulse is injected into the LVTSCR, and the measured I-V curve shows snapback characteristics during the short time. The snapback phenomenon of the LVTSCR device can be expressed by the fast transient simulation.

Figure 8 shows the comparisons of the vf-TLP measured curve with the simulated result. Comparisons of SPICE simulation results to vf-TLP measurement show a very good agreement both at low and high current regimes. The fluctuation of the high current region in the measured result comes from the limit of the high frequency measurements. Moreover, a very good correlation is achieved on the ESD key design parameters (Vt1, Vh, and Ron). Table 3 shows the deviation between the measured result and the simulated result with respect to key design parameters.

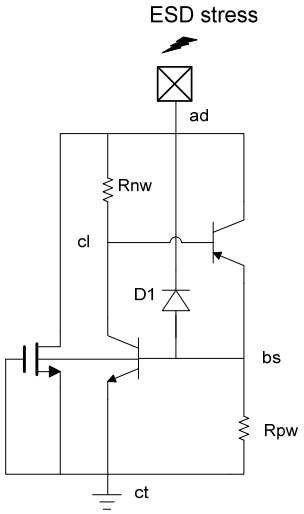

Figure 7: The equivalent circuit of this LVTSCR macro-model

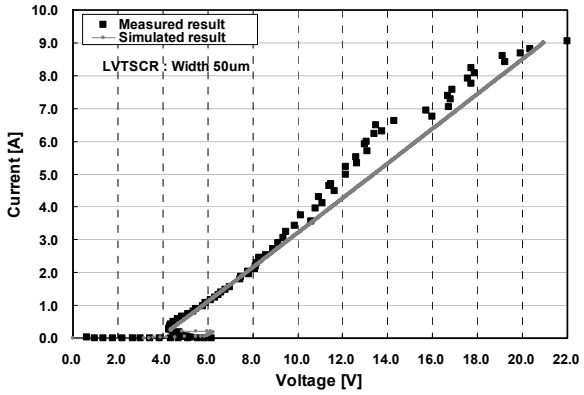

Figure 8: The comparisons of the vf-TLP measured curve with the simulated result

Table 3: The comparisons of the vf-TLP measured curve with the simulated result with respect to key design parameters

	Measured results	**Simulated results**	**%**
Vt1 [V]	6.2	6.2	0
Vh [V]	4.3	4.3	0
Ron [Ω]	1.9	1.9	0

5. Conclusion

In this paper, we reported the characterization and the behavior of a LVTSCR device with vf-TLP measurements. The results measured by the vf-TLP system showed that the triggering voltage (Vt1) is decreased, and the second breakdown current (It2) is increased in the comparison with the results measured by the standard 100ns TLP system. From the measurements on the devices fabricated using a 0.13 μm CMOS Process, it has been observed that the dV/dt effect and the power-to-failure versus pulse width relationship. The measurement result and the simulation data of the behavior approached model indicate a good correlation.

6. Acknowledgment

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7. References

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